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Lu, S., & Boussaid, F. (2015). A highly efficient P-SSH1 rectifier for piezoelectric energy harvesting. IEEE TRANSACTIONS ON POWER ELECTRONICS, 30(10), 5364-5369. [7084647]. DOI: 10.1109/TPEL.2015.2422717

Published in:
IEEE TRANSACTIONS ON POWER ELECTRONICS

DOI:
10.1109/TPEL.2015.2422717

Document Version
Peer reviewed version

Link to publication in the UWA Research Repository

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A Highly Efficient P-SSHI Rectifier for Piezoelectric Energy Harvesting

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Abstract—A highly efficient P-SSHI based rectifier for piezoelectric energy harvesting is presented in this paper. The proposed rectifier utilizes the voltages at the two ends of the piezoelectric device (PD) to detect the polarity change of the current produced by the PD. The inversion process of the voltage across the PD is automatically controlled by diodes along the oscillating network. In contrast to prior works, the proposed rectifier exhibits several advantages in terms of efficiency, circuit simplicity, compatibility with commercially available PDs, and standalone operation. Experimental results show that the proposed rectifier can provide a 5.8X boost in harvested energy compared to the conventional full wave bridge rectifier.

Index Terms—Piezoelectric energy harvesting, Parallel Synchronized Switch Harvesting on Inductor, AC-DC converter.

I. INTRODUCTION

Harvesting ambient vibration energy provides a means to extend battery operation and enable self-powered ultra-low power devices, such as wireless human body health monitoring sensors or medical implants (e.g. implantable heart assists) [1-3]. A piezoelectric device (PD) (Fig. 1) vibrating at or close to its resonant frequency can be modeled as a sinusoidal current source $i_p$ in parallel with its internal capacitance $C_p$ and resistance $R_p$ [3]. The ac signal produced by the PD needs to be rectified for most applications. Given that the amplitude of the current $i_p$ generated by the PD is low (within micro-amp range) [4], the efficiency of the rectification must be as high as possible.

![PD](Image 1 Equivalent circuit of a PD vibrating around its resonant frequency)

Conventional ac to dc rectification circuits for PDs include the full wave bridge rectifier (Fig. 2(a)) and the voltage doubler (Fig. 2(b)). Such circuits suffer from low efficiency due to the internal capacitance of the PD [4]. For the full wave bridge rectifier (Fig. 2(a)), the output current $i_p$ of the PD needs to charge (and discharge) the internal capacitance $C_p$ from $-V_{rec}+2V_D$ to $-V_{rec}+2V_D$ (or vice versa), before the current $i_p$ can actually flow to the output. This occurs every half cycle for the full wave bridge rectifier. In the case of the voltage doubler (Fig. 2(b)), the current $i_p$ cannot flow to the output every half cycle. This is because diode $D6$ is turned ON during the negative half cycle, with current $i_p$ flowing to ground. The shaded areas in Fig. 2 represent non-harvesting periods.

![Fig. 2](Image 2 (a) Full wave bridge rectifier and associated waveforms, (b) voltage doubler and associated waveforms)

The PD’s internal capacitance can be exploited to realize energy conversion input resonant circuits working synchronously with the vibration [5]. A well-known technique based on this approach is the Synchronized Switch Harvesting on Inductor (SSHI) technique proposed in [6]. In this technique, the PD is connected in parallel with a switch and an inductor. This technique is also called parallel SSHI (P-SSHI) (Fig. 3(a)). It operates as follows (Fig. 3(b)). At the beginning of every half cycle, the current $i_p$ produced by the PD changes polarity and the switch $M1$ is closed. As a result, the inductor $L$ and internal capacitance $C_p$ of the PD forms an oscillating network and the voltage across the PD is naturally inverted. This occurs without the energy generated by the PD being used to charge/discharge the internal capacitance $C_p$. A similar technique called series-SSHI (S-SSHI) (Fig. 4(a)) was proposed in [7]. Instead of connecting the switch and inductor in parallel with the PD, the switched inductor is connected in series with the PD. The
switch control strategy (Fig. 4(b)) is identical to that of the P-SSHI technique. When the current $i_p$ changes polarity, the switch M2 is closed and the energy stored in $C_p$ is transferred to the output capacitor $C_{\text{rect}}$ and the voltage across the PD is inverted through the rectifier bridge. The switch M2 is opened at the end of the inversion process, after which M2 remains opened until the next half cycle. The analysis presented in [8] shows that the performance of P-SSHI is better than that of S-SSHI, especially when the open-circuit voltage of the PD is low. To realize the P-SSHI or S-SSHI technique, there are four main implementation challenges associated to circuit complexity, compatibility with commercially available PDs, standalone operation and harvested energy. These are: (1) detecting automatically the polarity change of the current produced by the PD. This should occur every half cycle, with a frequency of vibrations typically lower than 300Hz; (2) controlling automatically the switch ON time to match the duration of the inversion process. The switch ON time, which is of the order of microseconds, should allow for the internal capacitance $C_p$ to fully discharge into the inductor, but no longer to avoid $C_p$ taking back energy from the inductor. In addition, given that the characteristics (e.g. $C_p$) of the PD may not be known, the switch ON time should not be preset to allow compatibility of the rectifier with different types of PD; (3) the resistance of the oscillating network should be kept at a minimum to help improve the inversion process of the voltage across the PD; and (4) keeping the total power consumption of all circuits lower than the harvested energy to ensure self-powered operation.

[4] proposed an implementation (Fig. 3(c)) of the P-SSHI technique, where switch M1 is implemented using two transistors. In this implementation, switch M1’s ON time is controlled by a digital inverter delay line. The latter is constructed using inverter chains including multiplexers. By applying different control words to the multiplexers, the delay line can be programmed to achieve different values of the ON time. However, the control words need to be generated externally and tuned to accommodate the internal capacitance of each specific PD. Another implementation (Fig. 3(d)) of the P-SSHI technique was presented in [5]. The rectifier uses two transistors (T3 and T4) and two diodes for switch M1. When the current $i_p$ changes polarity, the voltage signal generated by the passive differentiator changes polarity at the same time. The comparator’s output turns on transistors T3 and T4 at the beginning of every half cycle. In this implementation, the comparator needs both positive and negative voltage supplies. In [9, 10], we proposed to use comparators and logic circuits to control the switch ON time while alleviating the need for diodes along the switching path. Given that the switch ON time is of the order of several microseconds, the rectifiers in [9, 10] require circuits with very fast rise/fall times and thus relatively high energy consumption compared to the harvested energy. As a result, self-power operation was thus not achieved in [9, 10].

[9] proposed an implementation (Fig. 4(c)) of the S-SSHI technique. In this implementation, a displacement sensor and a processor are used for the synchronization and the generation of the switching commands. All of which need external power to run. [10, 11] implemented a self-powered S-SSHI (SP-SSHI) rectifier (Fig. 4(d)), which uses peak detectors to control the start of the switching time for the switch M2. However, there is always a phase lag between the peak voltage and the actual switching time. This is due to the voltage drops of diodes and transistors in the peak detector. Furthermore, this phase lag is larger for small vibrations than for large vibrations [12]. In order to eliminate the phase lag, the authors [12] designed a velocity control SSSI rectifier (Fig. 4(e)). This rectifier requires three PDs to vibrate synchronously. The first PD is used to provide power for the control circuit. The second PD is connected to a low pass filter that generates a signal to detect the polarity change of current $i_p$. The third PD is used for energy harvesting. This strategy results in a more complex and costly energy harvesting system. To address the above mentioned
limitations, this paper presents a simple yet highly efficient P-SSHI based rectifier. The proposed rectifier neither relies on displacement sensor, peak detectors, differentiator or filters to detect the polarity change of the current produced by the PD, nor does it rely on a DSP or processor to generate the required signals for the control of the ON time of the switch. Furthermore, the proposed rectifier only uses the harvested energy to power the control circuits, thereby alleviating the need for any additional power supply circuits. This paper is organized as follows. Section II describes the operation of the proposed rectifier and analyses the harvested and lost energy. Section III presents the experimental setup and results. A performance comparison between the proposed rectifier and reported implementations of the SSSI technique is discussed. Section IV concludes the paper.

II. PROPOSED RECTIFIER

The proposed rectifier is shown in Fig. 5(a). The voltages $V_p$ and $V_n$ at the two ends of the PD are used to detect the polarity change of $i_p$. Before time $t_0$, $i_p$ is positive, $V_p$ is close to $(V_{rec}+V_D)$ and $V_n$ is close to but lower than $-V_D$, where $V_D$ is the diode’s forward voltage. These two voltages are compared with $V_{ref}$, which is chosen slightly higher than $-V_D$. This is achieved using comparators CMP1 and CMP2. Since $V_p$ and $V_n$ are initially higher and lower than $V_{ref}$ respectively, OUT1 and OUT2 are low and high accordingly. At this time, the output of the NOR gate $N_{out}$ is low. When $i_p$ changes polarity from positive to negative at time $t_{inv}$, $V_n$ increases and reaches the value of $V_{ref}$. As a result, signal OUT2 changes from high to low while $V_p$ is still higher than $V_{ref}$ and OUT1 stays low. Therefore, $N_{out}$ changes from low to high. This latter change is used to detect the polarity change of $i_p$. When $i_p$ changes polarity again from negative to positive at time $t_{win}$, a similar process occurs. Subsequently, signal $N_{out}$ is processed to generate switching commands for transistors M1-M4. When $i_p$ changes polarity from positive to negative at time $t_{inv}$, the signals $\phi_1$ and $\phi_{1inv}$ are firstly generated. As a consequence, transistors M1 and M3 are turned ON and the oscillating network $Cp-L-D5-(M1, M3)$ is formed. Therefore, the voltage $V_I$ across PD is naturally inverted and this inverting process spans from $t_0$ to $t_1$. Control signals $\phi_1$ and $\phi_{1inv}$ are still high when the inverting process finishes, but diode D5 prevents the current flowing back, thereby terminating the inverting process. Subsequently, the current $i_p$ charges $C_p$ from $V_{inv} \rightarrow -(V_{rec}+2V_D)$ during time interval $[t_1, t_2]$ and then delivers power to the output. At time $t_{win}$, when $i_p$ changes polarity again, a similar process occurs for oscillating network $Cp-(M2, M4)-D6-L$. Fig. 6 shows the schematic of the clock divider, whose input is $N_{out}$ and outputs are $\phi_1$, $\phi_{1inv}$, $\phi_2$ and $\phi_{2inv}$. Input signal $N_{out}$ is a sequence of pulses, toggling from low to high at the beginning of every half cycle. A Divide-by-2 circuit is used to generate two groups of control signals for the two oscillating networks. This circuit is constructed using a D flip-flop with its complementary output connected to its D input and signal $N_{out}$ fed into the CLK input. Therefore, outputs Q and Q bar both have a frequency that is half that of signal $N_{out}$. D flip-flop’s output Q and Q bar are ANDed with a delayed version of signal $N_{out}$. As a result, signals $\phi_1$ and $\phi_2$ have the same pulse width than signal $N_{out}$ but half its frequency. $\phi_{1inv}$ and $\phi_{2inv}$ are the inverted versions of $\phi_1$ and $\phi_2$. 

![Fig. 5 (a) Implementation of the proposed rectifier and (b) associated current and voltage waveforms](image)

![Fig. 6 Clock divider](image)

As it can be seen from Fig. 4(b), the PD charges its internal capacitance $C_p$ from $V_{inv}$ to $(V_{rec}+2V_D)$ or $-V_{inv}$ to
\[-(V_{\text{rect}}+2V_D)\]. Therefore, the charge lost on \(C_p\) in the time interval \([t_1, t_2]\) is:

\[
Q_{Cp,\text{loss}} = (V_{\text{rect}} + 2V_D - V_{f,\text{invert}})C_p
\]  

(1)

where \(V_{f,\text{invert}}\) is the inverted voltage \(V_i\) at the beginning of every half cycle and is given by

\[
V_{f,\text{invert}} = (V_{\text{rect}} + 2V_D)e^{-\frac{\pi}{\sqrt{3}}} - V_D\left(1 + e^{-\frac{\pi}{\sqrt{3}}}\right)
\]  

(2)

\(Q\) is the quality factor of the oscillating network and is given by:

\[
Q = \frac{\omega}{\alpha}
\]  

(3)

where \(\omega = \sqrt{\omega_0^2 - \alpha^2}\), \(\omega_0 = \frac{1}{\sqrt{LC_p}}\) and \(\alpha = \frac{R_{\text{para}}}{2L}\). \(R_{\text{para}}\) is the parasitic resistance of the oscillating network.

Hence the charge lost on the \(C_p\) every half cycle is:

\[
Q_{Cp,\text{loss}} = (V_{\text{rect}} + 2V_D)\left(1 - e^{-\frac{\pi}{\sqrt{3}}}\right)C_p
\]  

(4)

\[+ V_D\left(1 + e^{-\frac{\pi}{\sqrt{3}}}\right)C_p\]

The charge lost on the internal resistance \(R_p\) every half cycle is

\[
Q_{R_p,\text{loss}} = \int_{t_0}^{t_\pi} \frac{V_i}{R_p} dt
\]  

(5)

In time interval \([t_0, t_1]\), \(V_i\) is inverted by the oscillating network and the length of this time interval is given by

\[
t_1 - t_0 = \pi \sqrt{\frac{L}{C_p}}
\]  

(6)

Since the time interval \([t_0, t_1]\) is very short compared to the half cycle of current \(i_p\), the energy lost in this time interval can be neglected. Then, in time interval \([t_1, t_2]\), the charge lost on \(R_p\) is:

\[
Q_{R_p,\text{loss}1} = \int_{t_1}^{t_2} \frac{V_{f,t_1-t_2}}{R_p} dt
\]  

(7)

and in this time interval, \(V_i\) is given by:

\[
V_{f,t_1-t_2} = \frac{1}{C_p} \int_{t_1}^{t} i_p \sin \omega t \, dt + V_f(t_1)
\]  

(8)

\[
= \frac{i_p}{\omega C_p} (\cos \omega t_1 - \cos \omega t) + V_f(t_1)
\]

The boundary condition for \(V_i\) is \(V_f(t_1) = (V_{\text{rect}} + 2V_D)e^{-\frac{\pi}{\sqrt{3}}}\) and \(\omega t_1 \approx 0\). \(V_p\) is the open circuit voltage of PD, defined as

\[
V_p = \frac{i_p}{\omega C_p}
\]  

(9)

hence,

\[
V_{f,t_1-t_2} = V_p(1 - \cos \omega t) + (V_{\text{rect}} + 2V_D)e^{-\frac{\pi}{\sqrt{3}}}
\]  

(10)

Bringing (10) back to (7), we obtain:

\[
Q_{R_p,\text{loss}1} = \int_{t_1}^{t_2} \frac{V_{f,t_1-t_2}}{R_p} dt
\]

\[
= \frac{V_p (\omega t_2 - \sin \omega t_2)}{\omega R_p} + \frac{(V_{\text{rect}} + 2V_D)e^{-\frac{\pi}{\sqrt{3}}}}{R_p}
\]  

(11)

where

\[
\omega t_2 = \cos^{-1}\left(1 - \frac{(V_{\text{rect}} + 2V_D)e^{-\frac{\pi}{\sqrt{3}}}}{V_p}\right)
\]  

(12)

In time interval \([t_2, t_3]\), the charge lost on \(R_p\) is

\[
Q_{R_p,\text{loss}2} = \frac{V_{\text{rect}} + 2V_D}{R_p} (t_\pi - t_2)
\]  

(13)

where

\[
t_\pi = \frac{\pi}{\omega}
\]  

(14)

The total charge produced by PD in every half cycle is:

\[
Q_{\text{total}} = 2C_p V_p = \frac{2I_p}{\omega}
\]  

(15)

Therefore, the harvested power for every cycle is

\[
P_{\text{harvest}} = 2f_p V_{\text{rect}}(Q_{\text{total}} - Q_{Cp,\text{loss}} - Q_{R_p,\text{loss}1} - Q_{R_p,\text{loss}2})
\]  

(16)

III. EXPERIMENTAL RESULTS AND DISCUSSION

The performance of the proposed rectifier was evaluated (Fig. 7) using a commercially available PD of dimensions 1.4x0.24x0.025 (inch) (V22B Mide Technology) mounted on a shaker (Labworks ET-126-B1). The shaker was excited at 225 Hz and driven by a sine wave generator (Labworks SG-135) amplified through a power amplifier (Labworks PA-138). The proposed rectifier was built using ultra-low power off-the-shelf ICs, Comparators CMP1 and CMP2 (Fig. 4(a)) were implemented using two ultra-low power ICs (LTC1540, Linear Technology, 680 nA max quiescent supply current). The NOR gate and the clock divider (Fig. 5) were implemented using Standard CD-4000 Series CMOS gates with low input current leakage. Switches along the oscillating networks were implemented using two types of MOSFETs (VN0104 and VP0104), with on resistance of 3 Ω and 11 Ω for a gate voltage of 5V, respectively. The diodes in the oscillating networks are Schottky diodes (BAT54) with a forward voltage of 0.2 V.

Fig. 8 shows the measured voltage waveforms across the PD and the output voltage \(V_{\text{rect}}\) for the proposed rectifier and full wave bridge rectifier. The measured waveforms are consistent with the operation waveforms shown in Fig. 5(b). As seen in Fig. 8(a), the inversion process occurs each time \(V_q\) or \(V_n\) reaches \(V_{ref}\). The control circuit can thus automatically detect the starting time of the inversion process. Note that the inversion process is not perfect with \(V_{f,\text{invert}}\lower than \(V_i\).
because of the parasitic resistance (from inductor L and switches) along the oscillating network. In Fig. 8(a), the current $i_p$ generated by the PD only needs to charge the internal capacitance $C_p$ from the inverted voltage $V_{invert}$ to the $\pm (V_{rect} + 2V_D)$, before charges can flow to the output. A significant amount of charges have thus been saved. This can be seen by comparing the amplitudes of the voltage $V_f$ in Fig. 8(a) and Fig. 8(b). With a 114.1 kΩ resistance attached to the output, the output voltage of the proposed rectifier can reach up to 2 V. In contrast, the full wave bridge rectifier could only provide an output voltage of 0.823 V. Fig. 9 shows the measured output power of the proposed rectifier (with different values of inductors) together with that of the full wave bridge rectifier as a function of the output voltage. The open-circuit voltage $V_f$ of the PD was set to 2.4 V. The curve at the bottom of Fig. 8 with triangle symbols shows that the full wave bridge rectifier’s maximum harvested power is 8.28 µW for an output voltage of 0.6 V. The middle curve with star symbols shows that the proposed rectifier (with a 22 µH inductor) can provide a maximum harvested power of 20 µW for an output voltage of 1.6 V. This maximum output power is 2.45X that of the full wave bridge rectifier. The top curve with square symbols is the output power of the proposed rectifier with a 940 µH inductor. This curve shows that the maximum harvested power of the proposed rectifier is 48 µW for an output voltage of 2.6 V. This value is 5.8X that of the full wave bridge rectifier.

Fig. 10 reports the output power of implemented externally powered and self-powered (by output voltage $V_{rect}$) rectifiers together with the power consumption of control circuits. The open-circuit voltage $V_f$ of the PD was set to 3.28 V. The output power of the self-powered rectifier is lower than that of the externally powered rectifier. The difference in the output power is the total power consumption of control circuits (blue bars in Fig. 10). When the output voltage $V_{rect}$ is less than 1.8 V, the control circuits are inactive, since this voltage is less than the minimum positive voltage supply requirement for the comparators. Table I compares the performance of the proposed rectifier against state-of-the-art SSHI implementations for piezoelectric energy harvesting. The
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